# Things to figure out:

* High level overview
* Avalon bus/stalls/timing logic
* How to execute each instruction, components needed for each
* Decide Verilog modules and assign them to people to implement and test

# Instructions and the components they use:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Instruction | Meaning | Equation | R, I, or J | Arithmetic/logic, jump/branch, or memory |
| ADDIU | Add immediate unsigned (no overflow) |  | I |  |
| ADD | Add unsigned (no overflow) |  | R |  |
| AND | Bitwise and |  | R |  |
| ANDI | Bitwise and immediate |  | I |  |
| BEQ | Branch on equal |  | J |  |
| BGEZ | Branch on greater than or equal to 0 |  | J |  |
| BGEZAL | Branch on non-negative and link |  | J |  |
| BGTZ | Branch on greater than zero |  | J |  |
| BLEZ | Branch on less than or equal to 0 |  | J |  |
| BLTZ | Branch on less than zero |  | J |  |
| BLTZAL | Branch on less than zero and link |  | J |  |
| BNE | Branch on not equal |  | J |  |
| DIV | Divide |  | R |  |
| DIVU | Divide Unsigned |  | R |  |
| J | Jump |  |  |  |
| JALR | Jump and link register |  |  |  |
| JAL | Jump and link |  |  |  |
| JR | Jump register |  |  |  |
| LB | Load byte |  | I |  |
| LBU | Load byte unsigned |  | I |  |
| LH | Load half-word |  |  |  |
| LHU | Load half-word unsigned |  |  |  |
| LUI | Load upper immediate |  |  |  |
| LW | Load word |  |  |  |
| LWL | Load word left |  |  |  |
| LWR | Load word right |  |  |  |
| MTHI | Move to HI |  |  |  |
| MTLO | Move to LO |  |  |  |
| MULT | Multiply |  |  |  |
| MULTU | Multiply unsigned |  |  |  |
| OR | Bitwise or |  |  |  |
| ORI | Bitwise or immediate |  |  |  |
| SB | Store byte |  |  |  |
| SH | Store half-word |  |  |  |
| SLL | Store left logical |  |  |  |
| SLLV | Store left-logical variable |  |  |  |
| SLT | Set on the less than (signed) |  |  |  |
| SLTI | Set on less than immediate (signed) |  |  |  |
| SLTIU | Set on less than immediate unsigned |  |  |  |
| SLTU | Set on less than immediate unsigned |  |  |  |
| SRA | Shift right arithmetic |  |  |  |
| SRAV | Shift right arithmetic variable |  |  |  |
| SRL | Shift right logical |  |  |  |
| SRLV | Shift right logical variable |  |  |  |
| SUBU | Subtract unsigned |  |  |  |
| SW | Store word |  |  |  |
| XOR | Bitwise exclusive or |  |  |  |
| XORI | Bitwise exclusive or immediate |  |  |  |

# Components:

## Instruction Decode Block

## ALU:

### Inputs:

* Input 1 (32-bit)
* Input 2 (32-bit)
* Instruction (32-bit)

### Outputs:

* Output (32-bit)

## PC:

### Input:

* Address (32-bit)

### Output:

* Next address (32 bit)

## Next instruction:

### Inputs:

* Instruction (32-bit)
* PC (32-bit)
* Register input 1 (32-bit)
* Register input 2 (32-bit)

## Output